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Analysis and Reduction of Simultaneous Switching Noise in Fast Integrated Circuits Using Ground-Reference Planes and Vector Fitting Method

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***Abstract*—This paper studies simultaneous switching noise (SSN) phenomenon in detail. The main objective of this work is the reduction of SSN. This is achieved firstly by adding the decoupling capacitors to check the paths impedance to ground and power planes. Then by using a proposed technique consisting to isolate the noisy components (digital circuits) of the sensitive components (analog circuits) by the addition of ground-reference planes with low noise. To analyze and quantify these different phenomena, the PSPICE simulations and the vector fitting method (VFM) are performed.**

***Index Terms*—Power Distribution Network, Simultaneous Switching Noise, Vector Fitting, Ground-reference planes, Matlab, Pspice.**

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I. Introduction

THE embedded system is an electronic system, which includes single microcomputer chip [1]. It configures to perform a specific dedicated application. This system is characterized by its high speed, its lower power dissipation, in addition to its smaller size and high frequency. But one of the problems encountered in these systems is the power integrity, which ensures that all components and transistors have a proper power supply and current that allow them to work in good operating conditions. So, designers should take into account all these elements to ensure the power integrity. Beginning at the receiving end of power distribution network (PDN), power is provided out of the ICs power connections by the multi-layer power grid. The power connection congenitally has non-ideals impedance at the latest results in a voltage drop at the transistors [2].

In general, PDN contains many networks of capacitors, inductances and resistors with several types and different values to obtain the impedance target on the frequency range required for ground-reference and power planes of PCB. The design of PDN interconnections should bear its impedance below the target impedance in the high frequency. This will be accomplished by three important principles of design [3, 4]. Although it may not always be possible to push it to the limit, it is always important to be aware of the constraints associated with the actual circuit. As a result, the most important principle to follow, for a profitable design, is to add an appropriate analysis in the design cycle. This will reduce the problems of design and the resulting product will present acceptable performance.

The power supply circuit of the current and voltage source is generally cumbersome and often cannot be directly connected to the transistors presented within the integrated circuits. The currents will therefore have to cross the interconnections of power/reference planes and bonding wires before feeding the transistors. All these elements have a resistance and an inductance and possibly a capacitance. The currents through these elements will therefore create voltage fluctuations at the arrival. Theses fluctuations are called the simultaneous switching noise (SSN). The SSN has many effects near the output of a chip owning to the following reasons [5]. The output drivers switch simultaneously at clock synchronized chips. Then, the outputs drivers, which are very large in size, need a significant amount of instantaneous current to switch and change their states. In addition to the parasitic inductance of the bonding wires in the range of nano-Henries. As a result, it is necessary to reduce the SSN to ensure smooth running of embedded systems.

Different methods have been proposed to reduce SSN, such as adding decoupling capacitors between power and ground-reference planes [6]. There are two primary purposes for using decoupling between power and ground-reference planes. The first purpose is for functionality, that is, the decoupling capacitor is a charge storage device, and when the IC switches state and requires additional current, the local decoupling capacitor supplies this current through a low inductance path. The second purpose for decoupling capacitors is to reduce the noise injected into the power and ground-reference plane pairs and thus reduce the emissions from the edge of the circuit board [7]. Another method to remove noise is the introduction of lossy components serving for the elimination of resonance based on the increase of the component loss [7,8]. Power islands are also used in the reduction of noise by isolating the components making noise on the power bus from sensitive devices [9].

Other method to mitigate SSN is to use the isolation moat [9] on the power or ground-reference plane or selecting the location of the via ports to eliminate the noise [10] at higher frequencies; these approaches are suitable only to suppress the

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noise at specific locations. Indeed, researches have proposed in [11, 12, 13] to use photonic bandgap or electromagnetic bandgap structure on the ground plane to form a high-impedance surface. Authors in [14] have also given a novel power/ground planes design using a low-period coplanar EBG structure (LPC-EBG).

This paper presents a study of SSN using decoupling capacitors and isolating noisy components (digital circuits) of the sensitive components (analog circuits) by the addition of ground planes.

This paper is organized as follows. Section 2 describes the problems of PDN, and the SSN reduction. In section 3, the method of vector fitting is explained and detailed. The results and discussions are included in section 4. Finally, conclusions are drawn in section 5.

II. Problems of power distribution network

The equivalent circuit of a basic power supply network is given by the Figure 1. On this circuit the Vdd voltage between power and ground planes, the load current source and the interconnections. The interconnections are represented by resistances and parasitic inductance Rp, Rg, Lp and Lg respectively. The presence of the current through the supply network impedance induced voltage drops. These variations of the voltages are called the power noise.

The electrical power noise affects the operation of the circuit by several mechanisms. The proper design of the charging circuit ensures a correct operation in accordance with the assumption that the power levels are maintained at an interval close to the levels of nominal voltage. This interval is called the noise margin of the power network.

The main objective in the design of the PDN is to give sufficient current for each transistor of the integrated circuit by ensuring that the power supply noise does not exceed the specified margins. Although, the noise power is a transient phenomenon corresponding to the switching transistors, the design of the PDN is accomplished in the frequency domain. This concept is the method most used by the designers. This method involves the PDN impedance optimization to respect the value of the target impedance. The greatest impedance for the PDN can be obtained by the high impedance that creates a voltage drop always below acceptable ripple specifications [15].

If the PDN impedance remains below the target impedance at each frequency, in the worst case of the supply voltage, the maximum of the transient current through this impedance will be lower than the fluctuations allowed. If the PDN impedance is very less than to the target impedance, this means that the PDN has been badly designed and will be more expensive.

A. Description of Simultaneous Switching Noise

Simultaneous switching noise (SSN) [16, 17], also referred in the literature as ground bounce, primarily occurs due to very large instantaneous power supply and ground currents propagating within a chip when many transistors are simultaneously switched between on and off states. The magnitude of SSN is found to be proportional to the parasitic inductor L associated

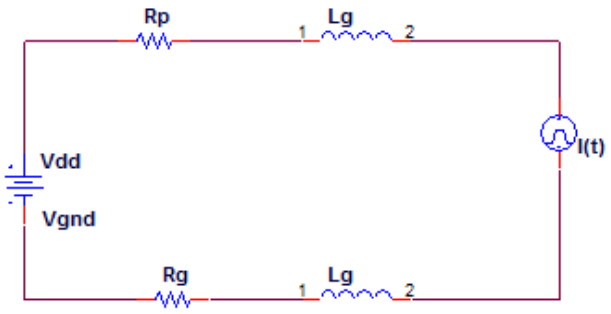

Fig. 1. The equivalent circuit of a basic power supply network

with power and ground networks along with the bonding wires that connect pads to pins, and the rate of change of the current through the inductor [18]. SSN noise often leads to serious degradation of signal integrity and overall performance of a chip. It generates glitches on the ground and the power-supply network, it decreases the effective driving strength of the gates, it causes output signal distortion impairing signal integrity, and it reduces the overall noise margin of a system. The effect of SSN is becoming more prominent because of the continuous increase in both chip integration level and system operating speed. Therefore, it is extremely important to accurately model the SSN to ensure high performance and reliable operation of VLSI chips.

The SSN can be calculated by several methods, such as assessing the peak by observing a negative local feedback [19], deriving an expression for peak value noise and assuming that this peak is a linear function of time during the output transition of the driver [20] or using a vector fitting method to give an approximation of the PDN impedance in the frequency domain [21,22].

B. Reduction of noise by adding the ground planes

Generally, the digital circuits are noisy and share the power in addition to the ground with analog circuits which are sensitive to noise. If many digital blocks switch simultaneously, the current draw of the distribution network can be significant. This important current pass through the parasitic resistance and inductance of the package, producing voltage fluctuations on the ground-reference planes. Therefore, it results the voltage variations at the analog circuits sensitive to noise. The figure 2 illustrates the conceptual diagram of two dominant coupling paths of the SSN to an analog chip on a SIP substrate [23, 24]. The path 1 is the path of the direct coupling propagation of the power supply to the analog chip through the PDN on-chip and on substrate SiP. The path 2 is the path of coupling SSN to the input signals of the analog integrated circuit through the transition was in the planes of common references of the substrate SiP. Indeed, by concentrating and basing on the elements of a mass plan, noise reduction can be done as indicated in the introduction.

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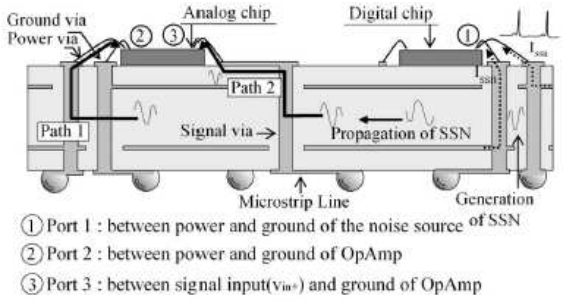

Fig. 2. The cross-section view of a SIP circuit describing two paths of the SSN noise of the digital circuit through the package of the substrate SIP to the analog circuit

III. Impedance characteristic of PDN by vector fitting

The PDN circuits become more complex, therefore the calculation of its impedance is not obvious. In fact, an approximation in the frequency domain is necessary. The principle of Vector Fitting consists to give a rational approximation of the impedance or the voltage in the frequency domain as shown in the equation (1).

$$\mathbf{Z}_{PDN}(s) \approx d + \sum_{n=1}^{N} \frac{r_n}{s - p_n} \tag{1}$$

Where s is the Laplace variable, p_n is the n-th pole, r_n is the residue corresponding to the n-th pole, N is the order of the rational function, and d is a constant [25,26,27].

The product of the equation (1) with an unknown function $\sigma(s)$; with known poles which we called weighting function; gives the equation (3).

$$\sigma(s) = \sum_{n=1}^{N} \frac{\overline{r}_n}{s - \overline{p}_n} + 1 \tag{2}$$

$$\sigma(s).Z_{PDN}(s) \approx \sum_{n=1}^{N} \frac{r_n}{s - \overline{p}_n} + d \tag{3}$$

Where $\overline{p}_n$ represent the poles of the function $\sigma(s)$ and $\overline{r}_n$ are the residues corresponding to $\overline{p}_n$.

By replacing $\sigma(s)$ by its expression we find:

$$(\sum_{n=1}^{N} \frac{\overline{r}_n}{s - \overline{p}_n} + 1).Z_{PDN}(s) \approx \sum_{n=1}^{N} \frac{r_n}{s - \overline{p}_n} + d \tag{4}$$

The equation (4) can be written as a linear problem that can be solved by the least squares method for k samples of frequency:

$$[A].\{x\} = \{b\} \tag{5}$$

Where:

$$[A] = \begin{bmatrix} \frac{1}{s_1-\overline{p}_1} & \cdots & \frac{1}{s_1-\overline{p}_N} & 1 & \frac{-Z_{PDN}(s_1)}{s_1-\overline{p}_1} & \cdots \frac{-Z_{PDN}(s_1)}{s_1-\overline{p}_N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \frac{1}{s_k-\overline{p}_1} & \cdots & \frac{1}{s_k-\overline{p}_N} & 1 & \frac{-Z_{PDN}(s_k)}{s_k-\overline{p}_1} & \cdots \frac{-Z_{PDN}(s_k)}{s_k-\overline{p}_N} \end{bmatrix}$$

$$\{x\} = \begin{bmatrix} r_1 & \cdots & r_N & d & \overline{r}_1 & \cdots & \overline{r}_N \end{bmatrix}^T$$

$$\{b\} = \begin{bmatrix} Z_{PDN}(s_1) & \cdots & Z_{PDN}(s_k) \end{bmatrix}$$

With:

$$k = 1, ..., N$$

The impedance function $Z_{PDN}(s)$ can also be written as:

$$\mathbf{Z}_{PDN}(s) = \frac{\prod_{n=1}^{N+1}(s - z_n)}{\prod_{n=1}^{N}(s - \overline{z}_n)} \tag{6}$$

The poles of $Z_{PDN}(s)$ have replaced by the zeros of $\sigma(s)$, $\overline{z}_n$. By Making several iterations the poles converge to constant values. By replacing the new poles into the equation (1), a new matrix equation (7) can be generated and solved with many samples of frequency, where the unknown parameters contain the coefficient d and r_n as:

$$\begin{bmatrix} \cdots & \cdots & \vdots & \cdots \\ 1 & \frac{1}{s_k-\overline{z}_1} & \cdots & \frac{1}{s_k-\overline{z}_N} \\ \cdots & \cdots & \vdots & \cdots \end{bmatrix} \cdot \begin{bmatrix} d \\ r_1 \\ \vdots \\ r_N \end{bmatrix} = \begin{bmatrix} Z_{PDN}(s_1) \\ \vdots \\ \vdots \\ Z_{PDN}(s_N) \end{bmatrix} \tag{7}$$

The vector fitting method (VFM) calculates the rational approximation of the PDN impedance in the frequency domain while respecting stability and passivity of the systems. The impedance in the time domain can now be easily obtained [22,25].

The rational approximation of the PDN impedance obtained in the frequency domain can be written as:

$$Z_{PDN}(s) = d + \sum_{m=1}^{M} \frac{a_m}{s - b_m} + \sum_{n=1}^{N} \frac{2r_{nr}(s - p_{nr}) - 2r_{ni}p_{ni}}{(s - p_{nr})^2 + p_{ni}^2} \tag{8}$$

The N poles, p_{nr}+jp_{ni}, p_{nr}-jp_{ni} and their corresponding residues r_{nr}-jr_{ni}, r_{nr}+jr_{ni} are complex conjugate pairs, and the M poles b_m and their corresponding residues a_m are real.

By using the inverse Laplace transform, the impedance in the time domain has obtained as follows:

$$z_{PDN}(t) = d\delta(t) + \sum_{m=1}^{M} a_m \exp(b_m t)h(t) + 2\sum_{n=1}^{N} \sqrt{(r_{nr}^2 + r_{ni}^2)} \exp(p_{nr}t) \cos(p_{ni}t + \varphi)h(t) \tag{9}$$

Where: $\delta(t)$ is the Dirac impulsion, *h(t)* is the unit step function and $\varphi = \arccos(\frac{r_{nr}}{\sqrt{r_{nr}^2+r_{ni}^2}})$.

It is clear that the impedance function in the time domain can be easily obtained from the rational approximation in the frequency domain.

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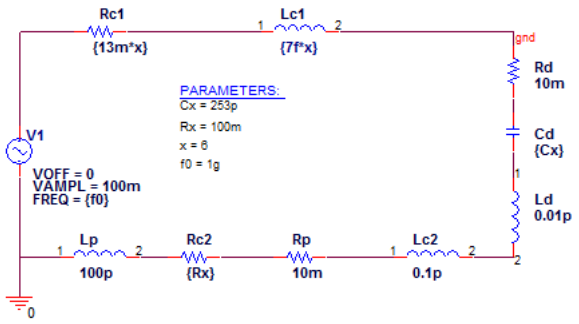

Fig. 3. The equivalent circuit of the noise reduction technique (ground plane)

IV. Results and Discussion

To study the effectiveness of the noise reduction on the ground-reference plane, a simplified model of the technique is used, as shown in Figure 3. The noise associated with the ground, induced by the simultaneous switching in the digital circuit, is modeled by a voltage source. The voltage source used is sinusoidal with amplitude of 100mV at a given frequency. The interconnections are modeled by R_p and L_p and the decoupling capacitor by R_d, L_d and C_d. The noise reduction technique between the noisy source and the receiver circuit (sensitive to noise) is based on the impedance of the ground path between the terminals (noisy circuit and sensitive circuit). This impedance is modeled by a RL circuit which is presented by R_{c1} and L_{c1} as shown in the figure 3. These elements are given by unit of length.

The maximum voltage on the ground victim is evaluated using PSPICE and VFM based on the distance (x) between the digital and analog circuits. The simulations are performed for x ranging from 1 to 10 (unit of length).

The ground noise reduction view by the circuit victim (analog circuit VQ_{gnd}) is represented as a function of the separation x as shown in the figure 4.

According to the Figure 4 we note that the noise reduction is about 52% which is reached for ten-unit lengths between the digital and analog blocks. The figure shows that when x increases, the noise decreases. Improved results can be achieved if the ground-reference plane impedance is smaller than the impedance between the sensitive circuits to noise and the noisy circuits.

The variations effects of the frequency f_0 of the noise signal as well as the decoupling capacitors C_d are simulated by the PSPICE tool and compared by VFM. It is considered that f_0 varies from 50% of the resonance frequency of the RLC circuit, and that C_d varies from 10% of the target value 253pF. These values are chosen for a typical CMOS technology. The effectiveness of the reduction of the ground noise for a sinusoidal noise source for several values of frequency and decoupling capacitors is illustrated respectively in figures 5 and 6.

Since the equivalent inductance of the ground plane between digital and analog circuits is not compensated, the noise surrounding f_0 is not much reduced.

As indicated in figure 6, the ground noise is weakly dependent of the decoupling capacitor C_d. In this technique the

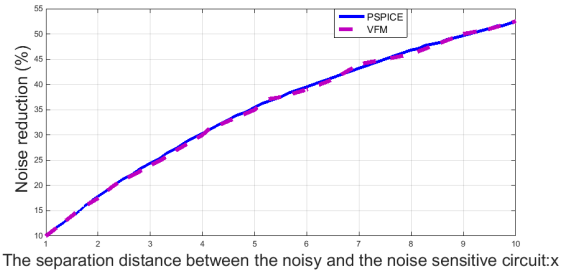

Fig. 4. The reduction of noise versus the separation distance between the circuit aggressors and the circuit victims

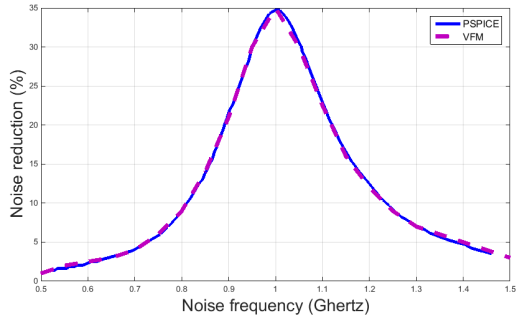

Fig. 5. The noise reduction for a sinusoidal noise source according to the frequency

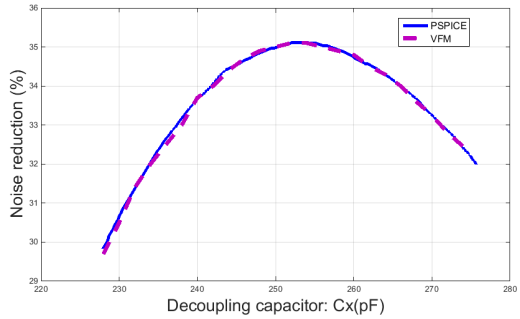

Fig. 6. The noise reduction for a sinusoidal noise source according to the decoupling capacitors

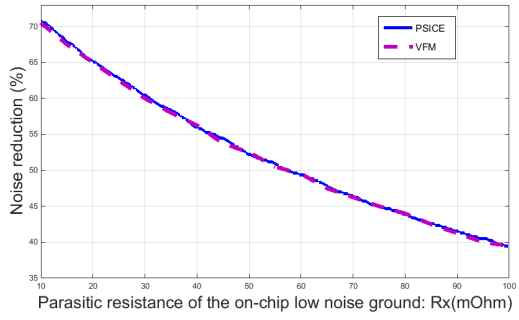

Fig. 7. The noise reduction for different values of the parasitic resistance of the ground plane

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noise is reduced by 4% over the range of C_d value.

The impedance of the ground plane added is purely resistive at the resonance frequency. The ground noise reduction and the ground-reference noise view of the circuit victim for several values of R_x are given by the figure 7.

The curves of the figure 7 show that the reduction of the noise may reach 70% for low values of R_x.

V. Conclusion

The establishment of a stable network power supply requires that the power planes impedance is lower than the target impedance. As an effect, it is necessary that the variation of the voltage does not exceed a specific level.

The interaction between the signal integrity and the power supplies integrity, also called the simultaneous switching noise (SSN), has been examined in detail on the complex and fast chip. The simultaneous switching will induce a significant voltage drop in the power. These simultaneous switching generates instability of the power planes and degrades the levels of the outputs of the transistors. The noise reduction technique proposed is to add a ground-reference planes between the digital circuit aggressor and the analog circuits sensitive to noise. The results obtained show the effectiveness of the technique used which helps to reduce the SSN and show also the coincidence of the two curves given by PSPICE and VFM.

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