Proceedings of Engineering & Technology (PET)
pp. 67-71

Study of SiC vertical-channel-JFET performances under limitation conditions

K. Shili [1], R. Gharbi [1].
[1] Laboratoire des Semi-conducteurs et Dispositifs Electroniques, C3S.
Ecole Supérieure d'Ingénieurs de Tunis.
05 Av. Taha Hussein, 1008 Montfleury, Tunis, Tunisia.
e-mail : rached.gharbi@esstt.rnu.tn
shilikhaoula18@yahoo.fr

M. Ben Karoui [1,2]
[2] Centre des Recherches et des Technologies de l'Energie.
Technopole Borj Cédria.
B.P N°95- 2050 Hammam Lif-Tunisia.

***Abstract*— The study of the dynamic behavior of the JFET Normally-off based on 4H-SiC (1200V-17A) will be presented in this paper. The evolution of the switching characteristics of the JFET has been studied and compared with the results found by simulation using PSPICE. According to the forms of experimental and simulation waves, we have able to extract the switching time: turn-on T_{on} and turn-off T_{off} which is low (of the order of 10^{-6}s) and still proves the rapidity of the switching speed of these transistors. But the influence of the many characteristic values limited the performance of this device and appears to be responsible for the failure.**

***Keywords*— JFET- SiC; switching characteristics; leakage current.**

I. INTRODUCTION

The potential of vertical JFET were highlighted especially for power applications and present themselves as good candidates for use in high temperature environments. They combine the quick switching of the unipolar transistors (eg MOSFETs), the ability to switch high current densities and the excellent thermal properties of the materials silicon carbide **[1] [2]**. The VJFETs are 100% unipolar which favors the parallel easier to switch high current of the order of hundreds of ampere **[3]**.

Thanks to the vertical structure of the channel, the SiC VJFETs allow greater integration density, very low on-state resistance and easier fabrication with low cost **[3] [4]**. Unlike the MOSFET, the SiC VJFET is based on the modulation width of the channel by the PN junction who prevents degradation of the component at elevated temperatures in the oxide gate of MOSFETs.

Several research projects are directed towards the best solution for reducing the switching losses: either reduces the switching frequency (which seeks to increase further to reduce the volume of components liabilities) or to reduce the switching time (fast semiconductors).

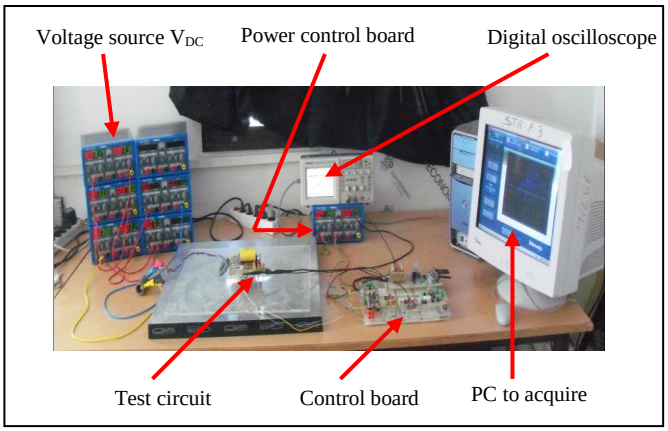
We will study a SemiSouth 1200V 17A SiC JFET **[5]** a vertical channel structure manufactured (VJFET), which is characterized by a very low state resistance, low gate charge and low intrinsic capacitance **[6]**. To fully exploit the potential of the SiC normally off JFET and to make sure that it can also be used in power electronic converters with high switching frequencies, the dynamic simulation of characteristics is given. The results are validated using experimental results under inductive switching conditions.

II. DESCRIPTION OF THE EXPERIMENTAL SETUP

A. Test Bench

The figure 1 shows the bench test used for measurement in commutation of the JFET Normally -Off (1200V -17A).

Fig. 1. Photograph of the test bench used for the measurement of switching JFET-SiC load RL



This circuit consists of a DC voltage source V_{DC}, the JFET transistor, a load resistor R and inductance L. The JFET transistor is voltage- controlled at its gate by a pulse voltage source. In practice there is a gate driver which was fixed resistance R_G and the supply voltage as function of test JFET. A control board generates the control signal driver.

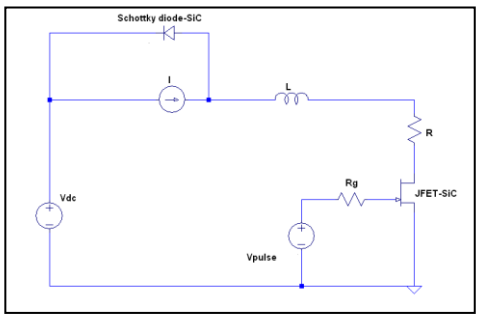
ISSN: 2356-5608

The dynamic experiments were performed at ambient temperature. Switching measurements were also performed at elevated temperatures (up to 100°C), but it was found that the switching waveforms at different temperatures were undistinguishable. For this reason only ambient temperature switching experiments are included.

B. The test circuit used in the simulation

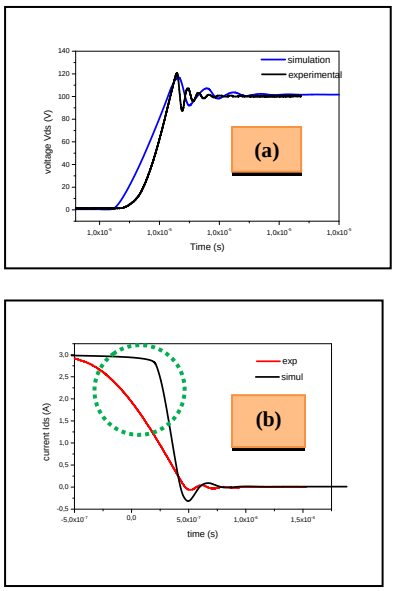
The model of the switching cell used in the simulation with PSPICE software is given in figure 2. We choose small values of R_g since it is advisable to avoid large gate resistors values with SiC components to avoid damaging their transient performance **[7]**. The specific resistance has a significant influence on the switching characteristic of the JFET.

Fig. 2. Switching test circuit used in the simulation of the SiC JFET.



The dynamic simulations were performed also using the specific on resistance model. It was found that the results were quite similar. That was expected, since switching waveforms are mostly affected by device capacitances.

Fig. 3. Experimental and simulation waveforms (a) of the voltage V_{DS} and (b) of the current I_{DS} in the opening of SiC-JFET.



The switching waveforms for our device are shown in fig. 3 ((a)-(b)). The experimental switching waveforms and obtained by simulation are comparable. Thus waveforms were a good indication of the excellent switching properties of the device. Considering the presented measurement results, the 1200V direct-driven SiC JFET is perfectly suited for use in photovoltaic inverters.

The table I summarizes the main parameters of our switching transistor, the oscillation frequency is order of 1MHz and presents a rise time t_r of the order of 640 ns and a fall time t_f of the order of 9 ns which its demonstrating the switching speed.

TABLE I. TRANSIENT PARAMETERS OF THE STUDIED JFET-SIC.

	I_d (A)	t_r (ns)	t_f (ns)	$t_{d,on}$ (ns)	$t_{d,off}$ (ns)	t_{tot} (ns)	f_{max} (MHz)
Experimental	3	640	9	275	15	939	1.065
Simulation	2.9	907	30	110	5	1052	0.95

According to the summary table of switch settings t-on and t-off show that the experimental results and those found by simulation are almost identical, the $t_{(on.exp)}$ is about of 275ns twice compared to that found by simulation $t_{(on.sim)}$ = 110ns, whereas the $t_{(off\ exp)}$ = 15ns and the $t_{(onsim)}$ = 5ns are closer.

Early switching, experimental decreases much faster pace than that determined by the simulation. This may be related to the inductive effect, the influence of the energy dissipated, where mainly the change of the temperature inside the chip, which is the physical cause of the failure. Other characteristic values appear to be responsible for the failure (such as the leakage current of the gate-source junction through the voltage drop in the gate resistor).

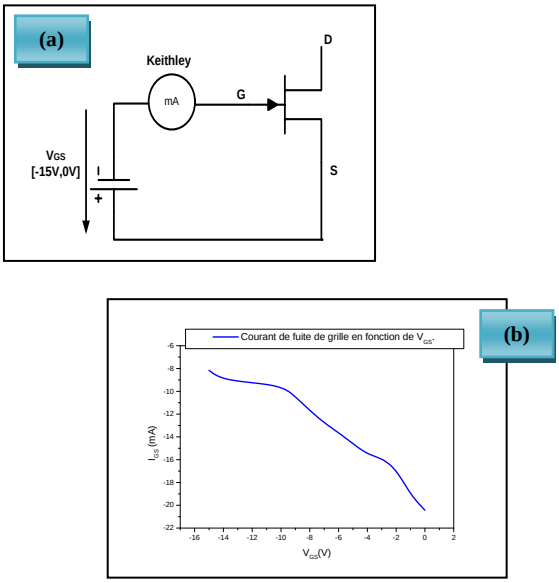
III. EFFECTS THAT ACCELERATES THE FAILURE OF SIC JFET

The VJFETs based on 4H-SiC (2A-600V) were studied by Merret **[8]**, with different voltages pinch V_{T0}. The devices are designed such that the threshold voltage may be positive or negative in decreasing or increasing the nominal width of the channel. Generally, more the JFET is conductive (ON), plus its specific resistance is low. On the other side, more the pinch-off voltage V_{T0} is negative, plus it will be necessary to have negative V_{GS} to pinch the channel especially at high drain voltage. The JFET Normally Off require only a very low gate voltage to block voltage but generally suffer from lower saturation currents compared to the Normally On, for a given gate-source voltage as we noticed in the case of our transistor. Merret et al. **[8]** tested the operation of this type of transistors at high temperatures up to 523K and the curves were extrapolated to 573K. In our case the transistor is tested up to 423K and we observed the same behavior, the saturation current of 6.4A to 4A decreases when the temperature

increases from 300K to 420K and this because of reduced electrons mobility with temperature. The results show that the drain current is 30% of 573K to 298K in the case of transistors tested by Merret compared with our transistors the drain current is 38% of the 300K to 420K. As for the leakage current in off state measured by the Merret, it has doubled in 298K to 573K but still acceptable even to 600V.

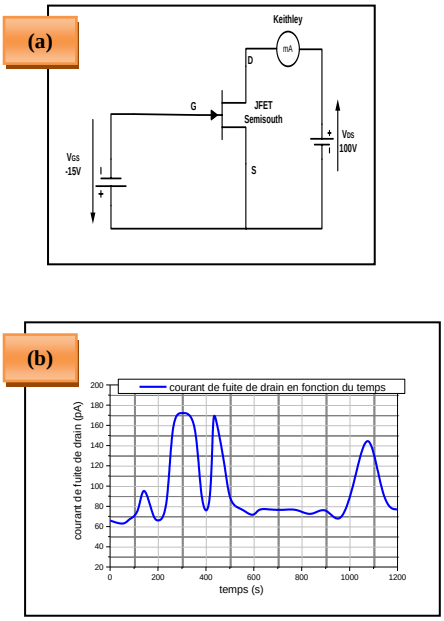
We tried to follow the evolution of the reverse leakage current of our transistor. The gate leakage current, I_{GS} is measured from the inverse characteristic of the junction gate source. The latter is treated as a reverse polarized diode that by applying a voltage V_{GS} ranging from -15V to 0V (with the Keithley SMU). The diagram block of the circuit characterization and evolution of the reverse current of the junction gate/source are represented in Figure 4. Monitoring of the evolution of the I_{GS} JFET can be an indicator of aging grid junction source and condition of the metal contacts at the gate and source.

Fig. 4. (a) Schematic diagram of the measurement of the gate current, (b) Evolution of the leakage current as a function of gate voltage V_{GS} of SiC JFET.



We also sought to estimate the leakage current when the JFET drain is blocked. We apply across the gate source junction voltage -15V. To measure very low intensities, we chose to perform these measurements using Keithley SMU. The applied drain-source voltage is limited to 100V, a value much lower than the breakdown voltage between drain and source of the transistor and which is 1200V. The evolution of the leakage current of SiC JFET drain (Figure 5(b)) shows that the current is very low (about 70 pA) and this peak (172 pA). This current could be an indicator of aging of the metal / semiconductor layer interface has been indicated by Moumen**[9]**.

Fig. 5. (a) Schematic diagram of the measurement of the drain leakage current, (b) Drain leakage current of the SiC JFET versus time (V_{DS} = 100 V).



We studied the switch performance of the JFET as function of the temperature. Cheng **[10]** studies the stability over time of the characteristics of VJFETs (8A-600V) in thermally stressful at room temperature 548K. The results show that the drain current decreases during the first few hours and then remains unchanged. We applied the same process on our JFETs in thermally stressful at T = 423K and we found that the drain current of 4.6A to 5A decreases after three hours and then stabilizes at this value. This reduction is higher drain voltage and higher gate. This may be related to the fact that defects in the material are driven by a strong electric field at high temperature, which affects the resistance in the on state and the depletion width of the channel. This result shows the advantage of JFETs with respect to MOSFET by eliminating the problem of movement of the load gate oxide for a long operation time.

IV. CONCLUSION

The study of 1200V-4H-SiC normally-off JFET showed the waveforms rich in information (f_{max} oscillation is 1.065KHz and a t_r is about 640 ns and a t_f in the order of 9 ns) which favors a better extraction of the dynamics parameters in modeling. Given the results measures presented, the JFET-SiC 1200V is perfectly suited for use in photovoltaic inverters and high temperature applications and high frequencies.

To highlight the importance and effects of changes in temperature on the JFETs Normally Off based 4H-SiC vertical structures, we sought to estimate, by experimental measurements, the leakage current between drain and gate as a function of temperature and linking such waveforms and the drain current observed when switching voltages, this to better understand the cause of the failure.

To retard degradation, solutions solder with intermetallic diffusion for the postponement chip / substrate have been implemented to improve the lifetime of the power components semiconductor, particularly for applications requiring higher temperatures operation.

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