NEW VARIABLE GAIN PI with NON-ENTIRE DEGREE for AC-DC CONVERTER with POWER FACTOR CORRECTION

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Abstract—This paper deals with a study and the application of a variable gain PI controller with non-entire degree (VGPI-NED). The considered system for application is an AC-DC boost converter with power factor correction (PFC). This system which is taken into account is the simple one without filter in entry by side grid. Starting by a classical PI controller, the VGPI one is realized then a controller with non-entire degree is proposed. The VGPI-NED coefficients are time-varying. This coefficients dependence on time is of polynomic type with a degree n, specially less than the unity. Simulation results show that the proposal is realizable and leads to good performances as tracking test, disturbance rejection with acceptable total harmonic distortion (THD).

Keywords—AC-DC converter, boost, PFC, THD, non-entire degree, PI, VGPI.

I. INTRODUCTION

Because of the proliferation of nonlinear loads which are related to the evolution of electronics, the laws which govern to limit their harmful effects on the network become more and more severe. The example can be shown by IEC 61000-3-2 for systems of class D [1]. Effectively, these kinds of load generate harmonic pollutions which lead, for example to a poor efficiency. Although, the conventional supply is of low coast, it generates the most harmonics on the network. The rated of re-injection may be quantified by the total harmonic distortion (THD). The power factor, F_p , is defined as follows:

$$F_p = P/S = V.I_1.\cos\varphi_1/V.I \tag{1}$$

With *P* and *S* denote respectively the active and apparent powers, *V*, I_l , *I* the rms values of the voltage, fundamental current and current, $\cos \varphi_l$, the displacement factor between fundamental current and voltage.

The expression of the current *I* is,

$$I = \sqrt{\left(\sum_{k=1}^{2} I_{k}^{2}\right)} = \sqrt{I_{1}^{2} + \sum_{k=2}^{2} I_{k}^{2}}$$
(2)

With I_k , the current of rank k.

The THD of current is defined as,

$$THD = \sqrt{\left(\sum_{k=2}^{2} I_{k}^{2}\right) / I_{1}^{2}} = (1 / I_{1}) \cdot \sqrt{\sum_{k=2}^{2} I_{k}^{2}}$$
(3)

According (1), (2) and (3),

$$F_p = \cos \varphi_1 / \sqrt{1 + THD^2} \tag{4}$$

The factor power F_p is thus related to the THD. With the current purely sinusoidal and in phase with the voltage, the factor power approaches the unit value ($F_p \approx 1$). Solutions to be adopted for the AC-DC boost converter with factor power correction are then summarized as follow:

- Obtaining a sinusoidal current network and in phase with the voltage
- Ensuring the smallest THD as possible in order to respect the standard normalize (for example, IEC 61000-3-2 for systems of class D)
- Ensuring voltage output constant.

In this paper, a classic scheme of a AC-DC converter without filters side the network is tested. The basic scheme is showed by Figure 1.



Fig. 1. Basic scheme of the AC-DC boost PFC

Two loops are here highlighted: the current loop and the voltage one. The interrupter K is here used for the load variation $(R_1 \rightarrow R_1/2)$. The current reference is obtained by

multiplying the output of the voltage controller with a party of the rectified voltage (K_{vr}, V_{rd}). The signal u(t) is used to control the static converter. This paper is organized as follows: first, the current loop is studied. The hysteresis command is chosen in this case. Some conditions are adopted to have a perfect loop in comparison with the voltage loop. The modeling of this voltage loop is then presented in order to permit PI controller tuning. The study of the VGPI-NED follows these generalities and simulations are used to verify various proposals.

II. CURRENT LOOP ANALYSIS

Usually, two kinds of controllers are used for the current loop: the PWM command and the hysteresis one. In this paper, the second kind is chosen. The method consists by forcing the current to remain between two sinusoidal envelopes max and min. The inductance of boost L must be so dimensioned according the chopping frequency F_d . The relation giving F_d according L is showed by (5) [2], [3], [4].

$$F_d = (1/T_d) = V_{rd} \cdot (V_s - V_{rd}) / (2.\Delta I \cdot L \cdot V_s)$$
(5)

With T_d is the period and ΔI , the imposed bandwidth of the current.

By (5), it is highlighted that in any time, the output voltage V_s must be higher than the rectified voltage V_{rd} . Fig.2 shows curves giving F_d according L for imposed ΔI . In this case, $V_s = 400$ [V], $V_{rd} = 235$ [V], $\Delta I = \pm 0.1$ [A] $\div \pm 0.3$ [A].



Fig.2. Frequency F_d according L.

III. VOLTAGE LOOP ANALYSIS

It can be considered that the current loop is faster than the voltage one. Then at every time, the reference current I_{ref} is assumed to follow well the rectified current I_{rd} ($I_{ref} \approx I_{rd}$). From this consideration, an approximated linear transfer function may be taken for the opened loop voltage [2], [4]:

$$\begin{cases} V_{s}(p) / I_{rd}(p) = V_{s}(p) / I_{ref}(p) = K / (1 + pT) \\ K = V_{M} . R / 4 . V_{s}; \quad T = R.C / 2 \end{cases}$$
(6)

Here V_M , V_s , R and C denote respectively the maximum value of the network voltage, the output voltage, the load resistance and the capacitor.

A. PI controller tuning

Two forms of PI function transfer are presented here:

$$\begin{cases} G_R(p) = 1 + pT_n / pT_i \\ G_R(p) = K_p + K_i / p \end{cases}$$
(7)

The first expression is used for the PI tuning and the second one to build the VGPI controller. Relations between of the different parameters are as follows:

$$K_p = T_n / T_i; \quad K_i = 1 / T_i$$
 (8)

Several methods are proposed for standard PID controllers [5], [6], [7],[8]. The transfer function of the opened loop of the voltage is:

$$G_0(p) = G_R(p).G(p) = [(1+pT_n)/pT_i].[K/(1+pT)]$$
(9)

The method consists to cancel the constant time dominant T and to impose the pole of the closed loop function transfer by the choice of the cut-of frequency F_c . Assume that, the constant time, $T_n = A$. T, (A is a constant positive) and by choosing A = I (*i.e.* the constant time T is cancelled), (10) can be established,

$$\begin{cases} T_{ni} = T \\ T_i = \frac{K}{2\pi . F_c} \end{cases}$$
(10)

Relation (8) gives then the parameters K_p and K_i .

B. The VGPI with non-entire degree (VGPI-NED)

The VGPI controller is built around the PI one. With the error e(t) taken as the input of the controller, the output u(t) is:

$$u(t) = K_p \cdot e(t) + \int_0^t K_i \cdot e(\tau) d\tau$$
(11)

The two parameters, K_p and K_i are defined as follow [9], [10], [11]:

$$K_{p} = \begin{cases} (K_{pf} - K_{pi}).(t/T_{s})^{n} + K_{pi} & \text{if } t < T_{s} \\ K_{pf} & \text{if } t \ge T_{s} \end{cases}$$
(12)

$$K_{i} = \begin{cases} K_{if} \cdot (t/T_{s})^{n} & if \quad t < T_{s} \\ K_{if} & if \quad t \ge T_{s} \end{cases}$$
(13)

Where K_{pf} and K_{pi} are the final and initial values of the gain K_p , K_{if} the final value of the gain K_i and T_s is the saturation time.

It may be noted that the initial value of the gain K_i is zero. The number n is defined as the degree of the VGPI. Usually, n is an entire number ($n \in \mathbb{N}$). The VGPI controller is presented by Fig. 3.



Fig. 3. Structure of the VGPI controller ($n \in \mathbb{N}$)

The step response of the VGPI controller is given by:

$$u(t) = \begin{cases} \left(K_{pf} - K_{pi} + K_{if} . t / (n+1)\right) (t / T_s)^n + K_{pi} & \text{if } t < T_s \\ K_{pf} + K_{if} . [t - T_s . n / (n+1)] & \text{if } t \ge T_s \end{cases}$$
(14)

For $n \in \mathbb{N}$ and $n \ge 1$, the step response follows a polynomial curve of degree (n+1).

If $t \ge T_s$ or n = 0, the PI and VGPI step responses are both linear and have the same slope K_{if} . It is clear that more n increases, more the step response is slower.

The variable gain PI with non-entire degree (VGPI-NED) is here considered when 0 < n < 1. The proposal is built by the observation given in (15):

$$\forall x \in \mathbb{R}, \ 0 < x < 1, \ \sqrt{x} > x \tag{15}$$

Fig. 4 shows the curves for the function: $y(x) = x^n$.



Fig. 4. Curves showing $y = x^n$

It is here highlighted that for 0 < x < 1, the function $y = x^n$ has always a higher value for n < 1. The reasoning rests then on the idea that the VGPI-NED step response chosen in this paper will be faster than the others where $n \ge 1$ because the step response follows a curve which looks like an exponential one. This property will be taken into account for the proposed VGPI-NED.

IV. APPLICATION ON A BOOST PFC

Here the AC-DC converter with power factor correction taken into account belongs to the system of class D. Fig. 5 shows the basic electrical scheme.



Fig. 5. Electrical basic scheme

Neglecting the voltage drop of the diode *D*, the modeling is resumed below:

$$\begin{cases} T = OFF, \ u(t) = 0, \ V_T = V_s \\ \Rightarrow V_{rd} - V_s = L.(di_{rd} / dt) \\ T = ON, \ u(t) = 1, \ V_T = 0 \\ \Rightarrow V_{rd} = L.(di_{rd} / dt) \end{cases}$$
(16)

According (16), relation between V_T and V_s is resumed as,

$$V_T = [1 - u(t)] . V_s \tag{17}$$

Because of the nonlinearity generated by the static converter T, a hysteresis command is used. It may be noted however that a method is proposed in using PWM without a needed modeling [12]. In this cited study, fuzzy logic controller (FLC) and the Lyapunov algorithm (LA) are adopted to control respectively voltage loop and the current one.

A. Simulation results

The PI controller tuning is done by fixing the cut-off frequency in closed loop. The final value of the parameter K_{pf} of the VGPI is higher than the PI's one. The initial value of the parameter K_{if} is taken equal to zero. The parameters of the controllers are calculated as follows:

$$\begin{cases}
PI: F_c = 5 [Hz] & K_p = 1,52 & K_i = 40,34 \\
VGPI: T_s = 3 [s] & K_{pi} = 1,52 & K_{pf} = 4,56 \\
K_{ii} = 0 & K_{if} = 40,4 \\
n = 1 & n = 2 \\
VGPI - NED: n = 0,3
\end{cases}$$
(18)

The condition tests are resumed below:

$$\begin{cases} t \ge 0 \ [s], \quad V_{sc} : 0[V] \to 400 \ [V] \\ t = 2 \ [s], \quad R : 328[\Omega] \to 164[\Omega] \\ t = 4 \ [s], \quad Vsc : 400 \ [V] \to 450 \ [V] \end{cases}$$
(19)

Here, the performances of the system with different controllers are appreciated by the test tracking, the disturbance rejection materialized by a severe variation of the load resistance and changing the set point. Figures 6 to 12 resume the simulation results.





Fig. 6. K_p and K_i curves for n = 0, 3 (a); n = 1(b) and n = 2 (c).



Fig. 7. Step responses with different values of the order n



Fig. 8. Current and voltage curves - current spectrum with n = 0,3.



Fig. 9. Current and voltage curves - current spectrum with n = 1.



Fig. 10. Current and voltage curves - current spectrum with n = 2.



Fig. 12. Zoom of transient behavior when $t > T_s$.

In Fig. 8 to Fig. 10, currents (in red) are multiplied by a factor 40.

B. Discussions

When the time *t* is higher than the saturation time T_s , all of the controllers have the same behavior because the gains are the same (K_{pf} and K_{ij}). Fig. 12 highlights this observation. The current spectrum analysis is adopted from t = 0,5 [s] with 5÷10 cycles; the frequency belongs to the interval [0, 5000 Hz]. All condition tests are the same to appreciate well the comparisons.

Table I resumes the performances obtained by the system with VGPI (n = 1, 2) and VGPIFO (n = 0, 3).

TABLE I. TERFORMANCES WITH VOFTAID VOFF	TABLE I.	PERFORMANCES	WITH	VGPI AND	VGPIFC
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Test	VGPI with different <i>n</i> and $T_s = 3 [s]$			
Test	n = 0,3	<i>n</i> = 1	<i>n</i> = 2	
$t > 0$ V $\cdot 0 \rightarrow 400$ [V]	$D_1 \approx 0\%$	$D_1 \approx 0\%$	$D_1 \approx 0\%$	
$l \ge 0$ V _{sc} . 0 7400 [V]	$t_{\rm M} = 0.6 [s]$	$t_{\rm M} = 1 [s]$	$t_M \ge 2 [s]$	
t = 2[s]	$\Delta V = 30 [V]$	$\Delta V = 30 [V]$	ΔV=32 [V]	
$R: 328 \ [\Omega] \rightarrow 164[\Omega]$	$\Delta t = 0,65 [s]$	$\Delta t = 0.9 [s]$	$\Delta t = 1 [s]$	
t = 4 [s]	$D_1 \approx 0\%$	$D_1 \approx 0 \%$	$D_1 \approx 0 \%$	
<i>Vsc</i> :400 [V] →450 [V]	$\Delta t = 0,5 [s]$	$\Delta t = 0,5 [s]$	$\Delta t = 0,5 [s]$	
THD	5,96 %	4,01 %	3,43 %	

Here t_M denotes the settling time or the rise time.

Fig. 7 and table I show that the VGPI-NED (here n = 0,3) step response is faster. All the controllers don't present any overshoot but the settling time (t_M) are not the same.

For the load resistance variation, it is highlighted that the VGPI-NED is better. The effect on the output is less significant and the duration of reaction time is shorter.

However, it can be remarked here that the THD with the VGPI-NED is the highest. It joins the conclusion that more the response is faster, more the THD is higher. The effect of the saturation time T_s may be noted. If T_s changes, for example, T_s is longer, all the step responses become slower but in every time, best results are always obtained with the VGPI-NED.

Now, a VGPI-NED with different values of the order *n* is discussed. The saturation time is kept unchanged. $(T_s = 3 [s])$. Figures 13 to 19 resume the simulation results.



Fig. 13 . System behaviors with VGPI-NED (n = 0,2; 0,3; 0,5)



Fig. 14. Transient behavior at load variation (n = 0,2)



Fig. 15. Transient behavior at load variation (n = 0,3)



Fig. 16. Transient behavior at load variation (n = 0, 5)



Fig. 17. Input current and voltage curves – Current spectrum with n = 0,2.





Fig. 19. Input current and voltage curves – Current spectrum with n = 0.5.

In Fig. 17 to Fig. 19, the currents (in red) are multiplied by a factor 40.

Table II resumes the performances obtained with VGPI-NED and with different values of the order n.

TABLE II. C	COMPARISON OF	VGPI-NED	PERFORMANCES

Test	VGPI-NED with different <i>n</i> and $T_s = 3 [s]$			
Test	n = 0, 2	n = 0, 3	n = 0,5	
$t > 0$ V $\cdot 0 \rightarrow 400$ [V]	$D_1 \approx 0\%$	$D_1 \approx 0\%$	$D_1 \approx 0\%$	
$l \ge 0$ V _{sc} . 0 7400 [V]	$t_{\rm M} = 0.5 [s]$	$t_{\rm M} = 0,6 [s]$	$t_{\rm M} = 0,70 [s]$	
t = 2[s]	ΔV= 29 [V]	ΔV=30 [V]	$\Delta V = 31[V]$	
$R: 328 [\Omega] \rightarrow 164[\Omega]$	$\Delta t = 0,5 [s]$	$\Delta t = 0,65 [s]$	$\Delta t = 0,70 [s]$	
t = 4 [s]	$D_1 \approx 0\%$	$D_1 \approx 0 \%$	$D_1 \approx 0 \%$	
<i>Vsc</i> :400 [V] →450 [V]	$\Delta t = 0,5 [s]$	$\Delta t = 0,5 [s]$	$\Delta t = 0,5 [s]$	
TDH	6,51%	5,96 %	5,08 %	

Fig. 13 shows that when the order *n* decreases, the step response starting from 0 [V] to 400 [V], is faster. With the VGPI-NED, there is no great difference on the output voltage when load variation $(R_1 \rightarrow R_1/2)$ is applied. However, durations of the reaction are different: the duration increases when the order *n* decreases. When the time *t* is higher than the saturation time $(t > T_s)$, the behavior is the same because each controller operates with the same gains K_{pf} and K_{if} .

According Table I and Table II, the settling time t_M increases with the order *n*. In every case, it is seen that more *n* decreases (the system is faster) more the THD increases. In every case, VGPI with non-entire degree leads to better results than the one with an entire order.

To finish the discussions, it is also useful to see the results obtained by the initial PI and the effects of varying the gains of the VGPI-NED.It is said above that the VGPI controller is built around the PI one. Here, variation of the order and using a higher multiplication factor λ to obtain K_{pf} and K_{if} are used. With a cut-off frequency F_c chosen above, ($F_c = 5$ [Hz]), (20) gives the parameters of the initial PI controller :

$$PI \begin{cases} K_p = 1,52\\ K_i = 40,34 \end{cases}$$
(20)

Here, the final value of the gain K_{if} is greater than the initial one (K_i) . Table III give some results.

TABLE III. COMPARISON OF PI AND VGPI-NED PERFORMANCES

	PI	VGPI-NED $T_s = 3 [s]$		
Test	$K_p = 1,52$ $K_i = 40,34$	n = 0,3 $K_{pf} = 3.K_p$ $K_{if} = 3.K_i$	n = 0,1 $K_{pf} = 3.K_p$ $K_{if} = 3.K_i$	
$t \ge 0 \ V_{sc}: 0 \rightarrow 400 \ [V]$	$D_1 \approx 0\%$ $t_M = 0.25 [s]$	$D_1 \approx 0\%$ $t_M = 0,2 [s]$	$D_1 \approx 0\%$ $t_M = 0.07 [s]$	
t = 2[s]	ΔV= 43 [V]	ΔV=27 [V]	$\Delta V = 27[V]$	
$R: 328 \ [\Omega] \rightarrow 164[\Omega]$	$\Delta t = 0,35 [s]$	$\Delta t = 0,25 [s]$	$\Delta t = 0,20 [s]$	
t = 4 [s]	$D_1 \approx 0\%$	$D_1 \approx 0 \%$	$D_1 \approx 0 \%$	
<i>Vsc</i> :400 [V] →450 [V]	$\Delta t = 0,25 [s]$	$\Delta t = 0,1 [s]$	$\Delta t = 0,07 [s]$	
THD	2,89%	6,11 %	6,99 %	

By Table III, it can be seen that the initial PI controller presents the less value of THD (2,89%). It is, on the contrary, mose sensitive by the effect of the load resistance variation.

The effect of selecting a high final value of K_{if} is here highlighted: it improves the speed regulation and reduces the effect of the load variation. But, in all cases, fast response is always accompanied by high THD.

Some remarks deserve to be emitted concerning the waveform of the output voltage V_s . Fig. 20 shows the zoom of V_s when the reference is $V_{sc} = 450$ [V].



Fig. 20 Zoom of the output voltage V_s

Relation (21) gives the approximative expression of the peak to peak value of the undulation ΔV_{pp} :

$$\Delta V_{pp} \approx \frac{V_s}{2\pi . R. f_e. C}$$
(21)

Here, R, C, f_e , V_s denote respectively the load resistance, the condensator value, the frequency of the input voltage side grid (here 50 [Hz]) and the ouput DC voltage.

With $V_s = 450$ [V], R = 160 [Ω], $f_e = 50$ [Hz] and $C = 470[\mu$ F], the results are :

- By (21), $\Delta V_{pp} = 19,04$ [V].
- By simulation, $\Delta V_{pp} = 20.8$ [V].

The two resultats are concordant. If the value of *C* increases, the magnitude of this undulation decreases. However, it should be noted that more the value of *C* increases, more the input current has an accentuated impulse form with a higher dephasing compared to the input voltage. It is also necessary to notice that the rippled component of the output voltage V_s has a frequency of 100 [Hz] (here $2^* f_e$). By the principle of the power-factor correction, this undulation cannot be eliminated without additionnal device inserted beside the output as filter or second DC-DC converter.

V. CONCLUSION

In this paper, a new VGPI controller with non-entire degree , called here VGPI-NED (0 < n < 1) is proposed to be applied

on an AC-DC converter with power factor correction. The controller tuning starts from a classic PI one to built the VGPI controller then the order or degree n is chosen as non-entire, specially with condition 0 < n < 1.

Simulation results show that this controller leads to better performances as tracking test, load disturbance rejection in comparison with the VGPI with entire order. The saturation time and the different gains have an effect of the step response speed and specially, on the THD: there is always a dilemn and their choice depends consequently on the desired performances. Studying the optimization to choose the best combination of these three parameters, K_{pf} , K_{if} and T_s seems interesting.

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