International Journal of Scientific Research & Engineering Technology (IJSET)
ISSN: 2356-5608, Vol.3, issue 3

CMOS Sensor Technology and SPICE Simulation of Sensing Circuits

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Abstract— **This paper describes a VLSI design project on CMOS image sensor chips. It shows architecture, colour filter mosaic array, active pixel sensor photodiodes, photodiode APS, sampling circuit and voltage-current conversion circuits. A simplified circuit structure and SPICE simulations have been done for sensing circuit. A single-stage OTA (Operational Transconductance Amplifier) design is also described and simulated for low voltage sigma-delta ADC applications.**

Keywords— **CMOS image chip, DSM, sensing, current-voltage conversion, circuit, Sigma-Delta ADC, OTA, low-voltage, low power, SPICE simulation.**

I. INTRODUCTION

An image sensor is a device that converts an optical image into electronical signal. It is used mostly in digital cameras, smart phones, camera modules and imaging devices. It contains a bayer colour filter mosaic array and underlying active pixel sensor photodiodes. It also contains analog-to-digital conversion, analog signal processing, clock and timing control. Digital logic circuits include interface, timing, processing and data output. Fig. 1 shows underlying CMOS active pixel sensor (APS) photodiode structure in CMOS image chip [1]. It contains photodiode on silicon substrate and potential well. It also contains column and row select buses, reset transistor, amplifier transistor, microlens and red colour filters.

Major advantage of CMOS image sensor is to integrate processing and control functions directly in VLSI technology. Active pixel sensor (APS) architecture includes both photodiode and read amplifier in each pixel. This will enable charges accumulated by photodiodeto be converted and amplified intovoltages in the pixel. Voltages arethen transferred through rows and columns to signal-processing unit. Among different ADCs, sigma-delta ADC is the most suitable for high-resolution applications due to higher linearity, which is achieved by using linear quantizer and oversampling technique. However, non-idealities in building blocks still strongly affect ADC output performance. Scaling of CMOS technology makes non-idealities even more severe. The most important constraint is the distortion problem in high-resolution sigma-delta ADCs. The continuallydecreasedsupply voltage in low-power applications results inmore performance degradation[1].

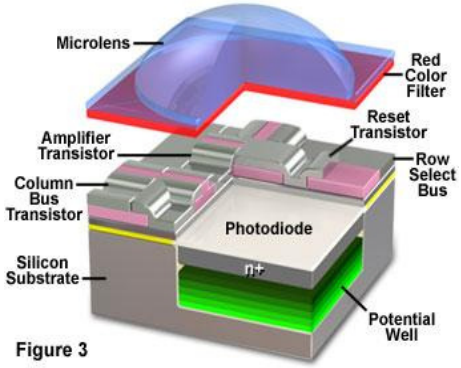

Fig. 1APS (Active Pixel Sensor) Photodiode Structure [1].

This paper is organized in the following sections. Section I is the introduction about image sensor CMOS technology. Section II describes APS (active pixel sensor) and sampling circuits. Section III presents SPICE simulation results on sensing circuit. Section IV describes a single-stage OTA (Operational Transconductance Amplifier) design and Spectre simulations are reported for AC, DC and transient analyses. Section V gives conclusions and future Internet applications using image sensor chips.

II. APS AND SAMPLING CIRCUIT

In sigma-delta modulation CMOS imager, analog signals from APS photodiodes are sensed to DSM sensing circuits. Outputs from DSM sensing circuits go thorough digital counters to output digital codes. Fig. 2 shows APS sampling schematic. Device M1 works as reset switch. M2 is a source follower. M3 performs as row select switch. A currentsource is used to discharge parasitic capacitance.When ResetN and RowN are high, pixel reference voltage VR is placed on column line as shown in Fig. 3. At this time sample and hold reference signal, SHR, goes high and VR is sampled onto a hold capacitor as shown in Fig. 3. In the next state, ResetN goes low and photodiode changes the light into charges. After

the aperture time, the information from photodiode is on the column line. VI is then sampled and held on a held capacitor when signal SHI goes high.

Fig. 4 shows the schematics of current conversion and subtracting circuits. We take difference of currents according to a current mirror. The current corresponding to reference voltage is calculated as follows:

$$I_R = \frac{VDD - V_{THP} - V_R}{R_R} = \frac{V_{R,shift}}{R_R}$$

The current corresponding to intensity of the light is calculated as follows:

$$I_I = \frac{VDD - V_{THP} - V_I}{R_I} = \frac{V_{I,shift}}{R_I}$$

So difference in these currents is summed in the bucket capacitor.

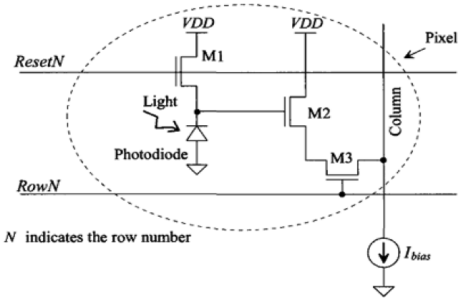

Fig. 2 APS Sampling.

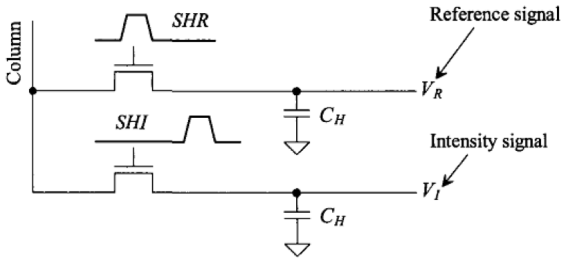

Fig. 3Reference and Intensity Signals.

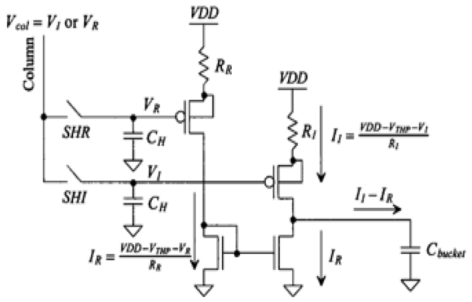

Fig. 4 Current Conversion and Subtracting Circuits.

III. SENSING CIRCUIT AND SIMULATION

Fig. 5 shows sensing circuit used in CMOS image chip. We use Spice circuit simulation tool to simulate the sensing circuit. V_I and V_R are varied in simulations to observe the stability of output signals. The circuit is able to sense about 500ns in voltages V_I and V_R based on simulation waveforms.Table I lists simulation results with three V_I voltages in the following equations:

$V_{I,\ shift} = VDD - V_{THP} - V_I$;

$V_{R,\ shift} = VDD - V_{THP} - V_R$.

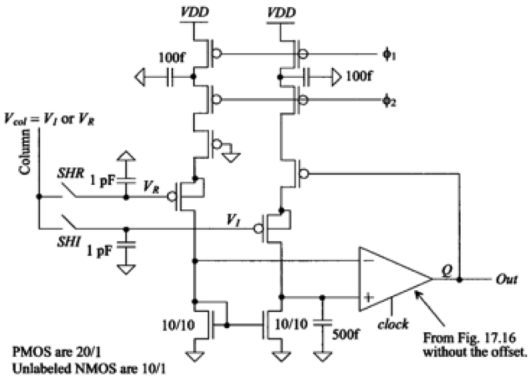

Fig. 5SignalsSensing Circuit.

TABLE I

SIMULATION RESULTS OF SENSING CIRCUIT.

	Simulation I	Simulation II	Simulation III
V_I	650mV	645mV	400mV
V_R	650mV	650mV	650mV
$V_{I,\ shift}$	100mV	105mV	357mV
$V_{R,\ shift}$	100mV	100mV	100mV

IV. SIGNLE-STAGE OTA DESIGN

Being the most important building block in analog sensing circuits, the amplifier faces difficulty in the low-voltage design, providing high gain and reasonable output swing while for low-power consumption. The intrinsic gain of the transistor is usually lower than 20dB. A usual way to boost the gain, cascoding of transistors, is not available in low-voltage design due to its output swing limitation. Alternatively, cascading transistor, i.e. the multi-stage amplifier, is possibly adopted. However, a cascade structure, which boosts gain with more than one amplifying stage, normally increases the power consumption and needs the frequency compensation. These constraints lead to the most power efficient solutionsingle-stage amplifier without cascading in our investigation.

International Journal of Scientific Research & Engineering Technology (IJSET)
ISSN: 2356-5608, Vol.3, issue 3
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Specifications of the sigma delta ADC for which OTA has been designed aregiven as follows.The dynamic rangeDR = 65 dB; input frequency: 10 kHz; ADC sampling rate: Fs = 20 KHz and maximum voltage: 1.2V in a 130nm process library. Based on the dynamic range, ADC resolution can be calculated as (DR – 1.76)/6.02 = 11 bits. Number of ADC quantization levels is required as 2^(Resolution of ADC) = 2048, OSR = 32, sample time 1/(Fs*OSR) seconds = 1.5625 * 1e-6s and clock frequency (Fs * OSR) = 32*20 KHz or 640 KHz.

Another sigma-delta ADC design perspective is that the gain of OP amplifier should be higher than OSR. GBW (Gain Bandwidth Product) should be higher than product of OSR and ADC sampling frequency. The gain requirement is not very high in our design, since OSR is only 32. Single-stage current mirror OTA (Operational Transconductance Amplifier) fulfils the above requirements and makes it a good candidate for low-power low-voltage amplifier design [2]. There is no need to go for multi-stage OTAs and also no compensation is needed. The schematic of the single-stage OTA design is shown in Fig. 6.

Fig. 7 shows DC analysis of the OTA design. The offset of OTA was set to 600mV i.e. half of full voltage range allowed in the design. AC analysis showed the gain of OP Amp is around 30, which is pretty close to OSR value 32 as shown in Fig. 8. The bandwidth was found around 2.3 MHz which was well above 32*20KHz = 640KHz requirement. The phase margin was 83 degrees. Hence, this OTA design was found to be satisfactory.

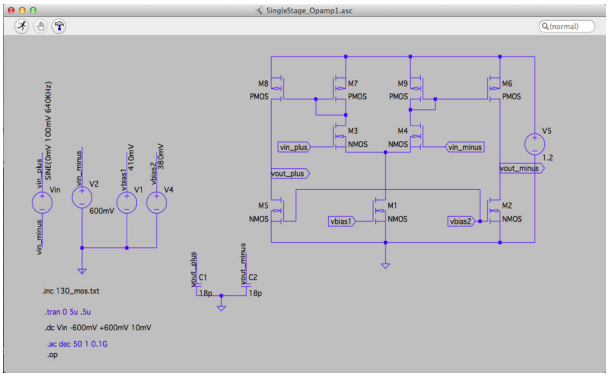

Fig. 6 One-Stage OTA Schematic.

Fig. 9 shows the transient analysis simulationresult. For input sine wave amplitude, amp =100 mV, output is a perfect sine wave; for amp = 150 mV, output has a minor distortion at the peak; for amp = 250 mV, output still has a sine format, and for amp > 250 mV, the distortion increases.Fig. 10 shows the schematic of OTA. Fig. 11 shows the setup made to simulate OTA. Table 2 shows rise/fall time based on simulations. It works for the input frequency 640 KHz. The single stage current mirror OTA is satisfactory for low-voltage sigma-delta ADC applications.

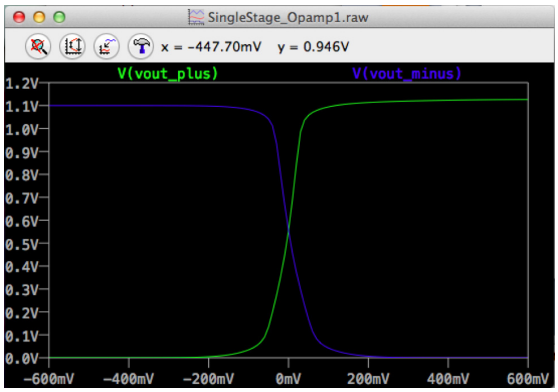

Fig. 7 DC Simulation.

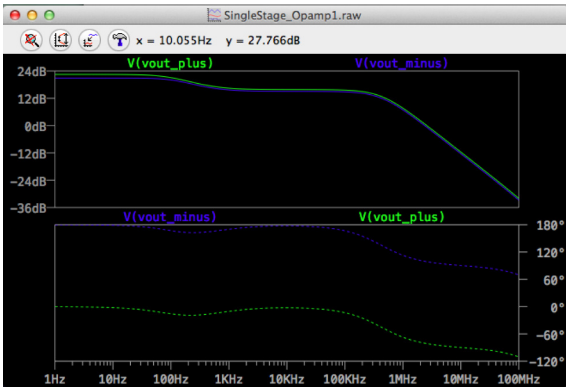

Fig. 8 AC Simulation.

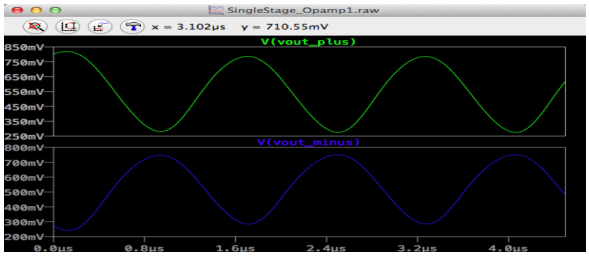

Fig. 9 Transition Analysis.

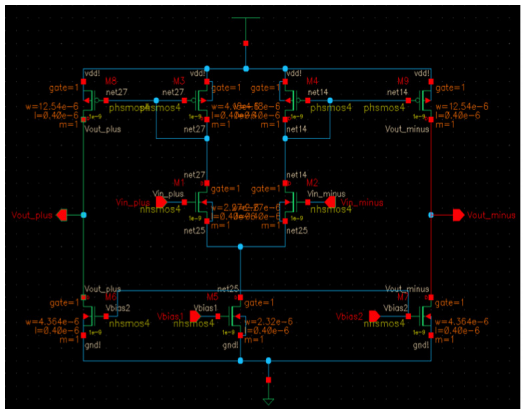

Fig. 10 OTA Schematic.

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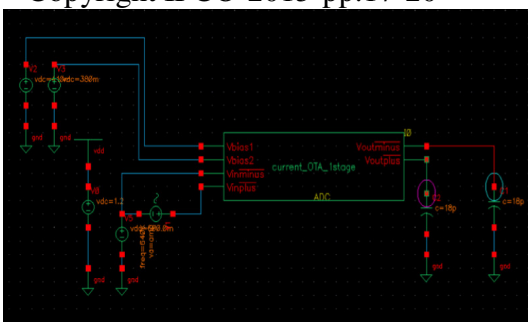

Fig. 11OTA Stimulus Setup.

TABLE II
RISE/FALL TIME OF OTA OUTPUTS.

	Vout_plus	Vout_minus
Rise time	293.54ns	328.85ns
Fall time	264.56ns	287.20ns

V. CONCLUSIONS AND APPLICATIONS

CMOS image sensor chip technology becomes popular due to continued integration in the CMOS process. In this paper, we describe a CMOS image sensorproject. It shows architecture, colour filter mosaic array, active pixel sensor photodiodes, photodiode APS, sampling circuit and voltage-current conversion circuits. Simplified circuits and SPICE simulations have been done for sensing circuit. Single-stage OTA (Operational Transconductance Amplifier) is described and Spectre simulations are reported for AC, DC and transient analyses. Performance and stability are satisfactory for low-voltage sigma-delta ADC design. Among different analogue-to-digital (ADC) converters, sigma-delta ADC is the most suitable for high-resolution applications. Main efforts are optimizing non-idealities in the sigma-delta ADC circuit.

Many technically challenging issuesstill remain to apply CMOS image chips in low-power, high-density and low-cost applications. Photodiodes and detectors are key to improve the resolution, accuracy, size and low-cost integration in image chips. Triple-well photodiodes technology can reduce leakage current and improve the stability [11].Other techniques including dual-Vt, dual-oxide-thickness devices as well asFinFET transistors are used toreduce the leakage current especially in mobile applications [12].

CMOS image chips are in the strong demand for Internet applications, as shown in Fig. 12. For example, we can build smart city environment with the following Internet-and-sensor applications [13]:

- *Smart parking* to monitor parking spaces available.
- *Noise maps* to monitor sounds in city.
- *Electromagnetic field levels* to detect energy radiated in cells and WIFI routes.
- *Smart helath* to detect available health cares and hospital facilities.
- *Smart lighting* to use intelligent and weather adaptive lighting in streets and areas.
- *Waste management* to detect rubbish levels in containers.
- *Smart traffic* to detect routes, congestions, climate conditions and unexpected events such as accidents and traffic jamson roads.

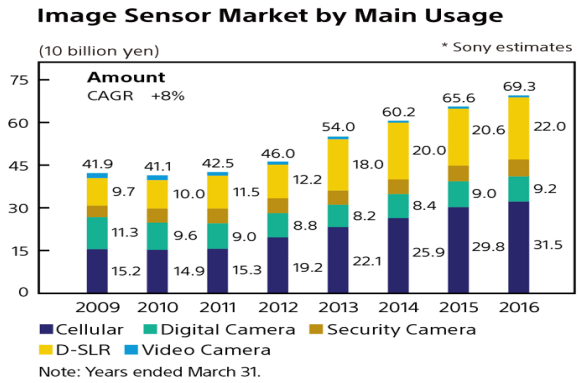

Fig. 12 MarketGrowth of Image Sensor Chips.

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